고정밀 시편 전처리를 위한 밀링 장비를 소개합니다.

Package and Die Level Deprocessing

X-PREP®

X-Prep® Precision Milling/Polishing System

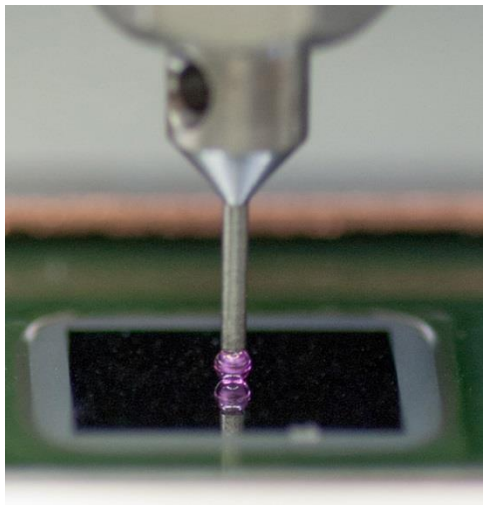
X-Prep® Vision™ - Substrate Measurement Instrument

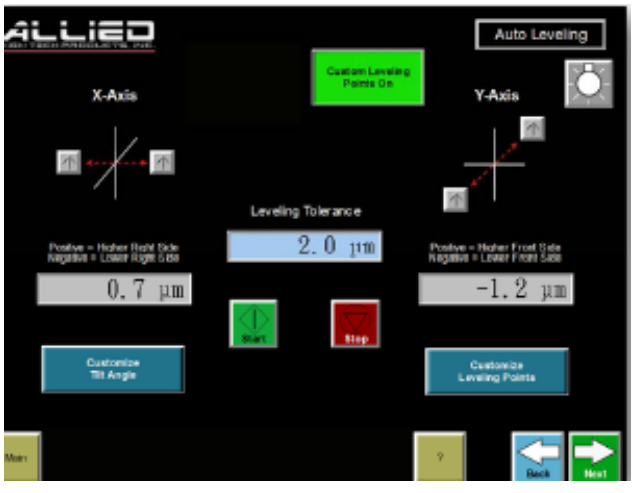
- 자동 샘플 레벨링(Automatic Sample Leveling)

→ 최소 0.5um 오차 평면성 조절 가능

- 오목(Concave)/ 볼록(Convex) 3D형태의 Parallel Polishing 진행 가능

- Si Thickness 측정을 통한 Thinning 작업 가능





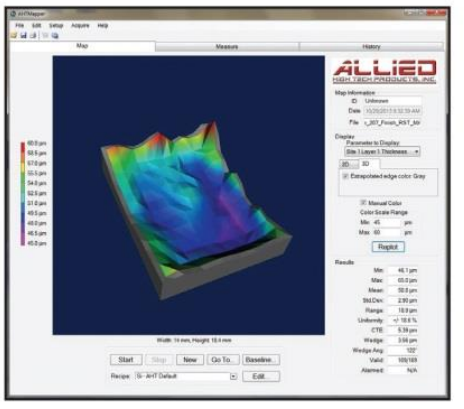
Example of results using X-Prep® Vision™

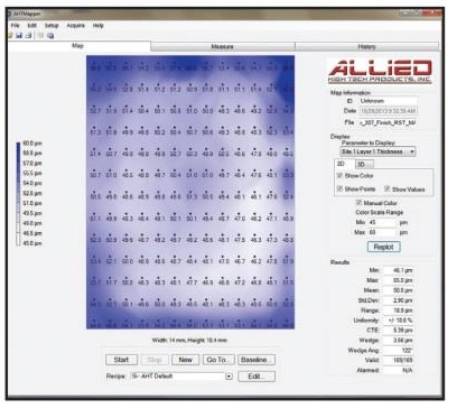
Backside

-CSAM / FIB / LADA / LIVA / LVP / OBIC
OBIRCH / PEM / SIMS / TIVA / VLVP

3D TSV – Stacked Die

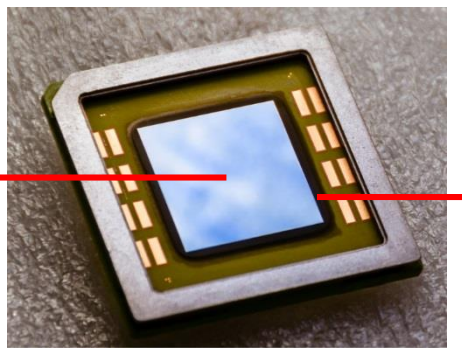
- Flip-Chip - GPU
- NAND/Flash memory
- SoC, PoP, and SiC

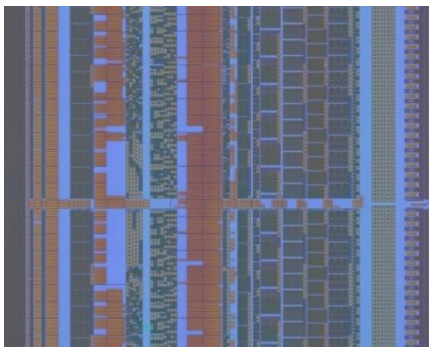




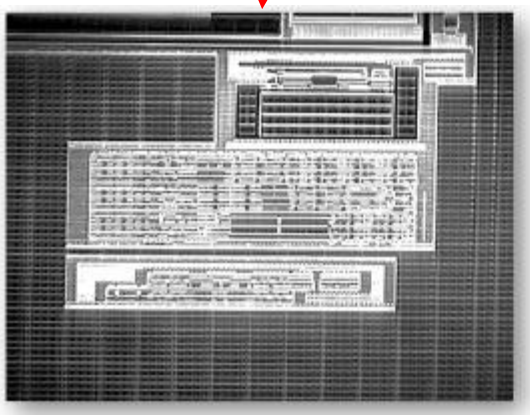
Both 3D & 2D Data Provided

Uniform flip-Chip Silicon Thinning

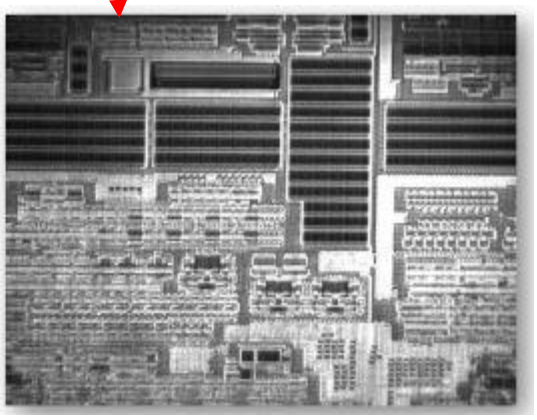




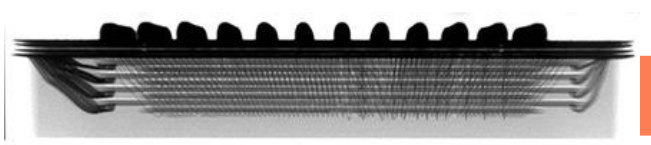
After removing Si and exposing the Gate Mag: 500X



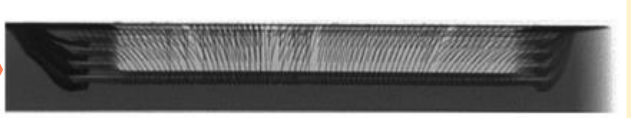
High NA SIL images show center (left) to edge (right) uniformity



Stacked Die Deprocessing



Stack Die X-ray 이미지



Stack Die Deprocessing X-ray 이미지

Example of results using X-Prep®

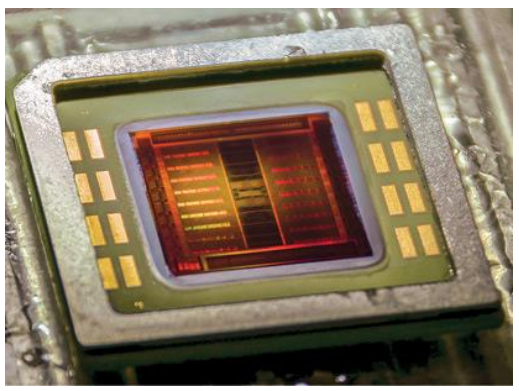
Front-Side
-Decapsulation
-Delayering/deprocessing/reverse engineering

Processors
- Hybrid Super SoC's
- WL/CSP – Wafer and chip
- 2.5D Devices – FPGA

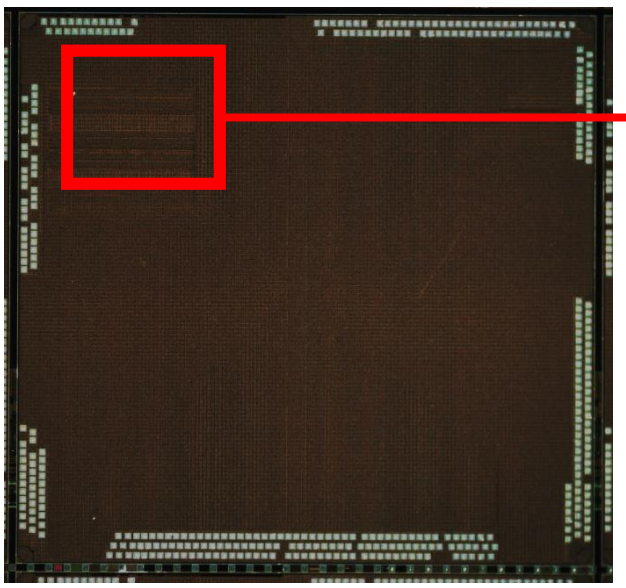
Lead – Frame
- TSOP – Thin small outline package
- SSOP – Shrink small outline package
- SOIC – Small outline IC
- DIP – Dual inline package

Leadless – Quad
- PLCC – Plastic leaded chip carrier
- QFN – Quad flat no-lead
- QFP – Quad flat package

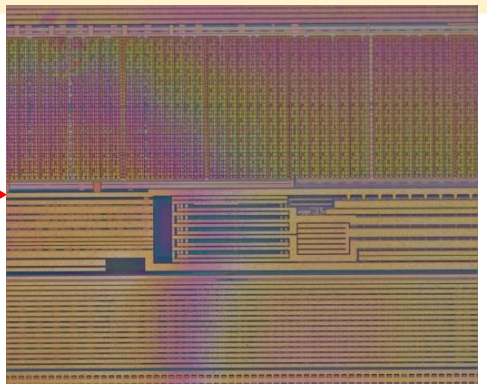
Front Side Die Delayer



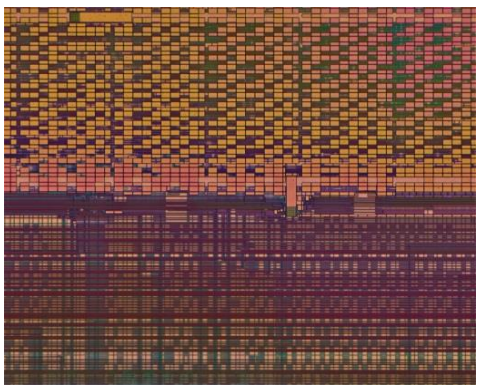
After removing passivation and exposing



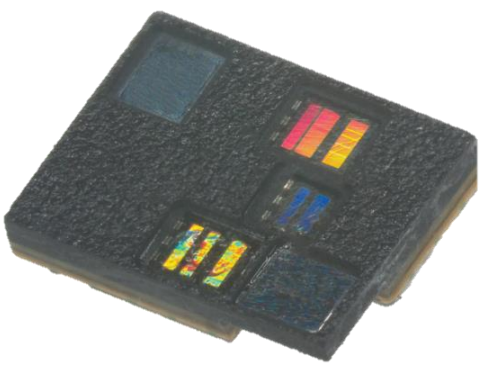
Sample type : Cu layer Die



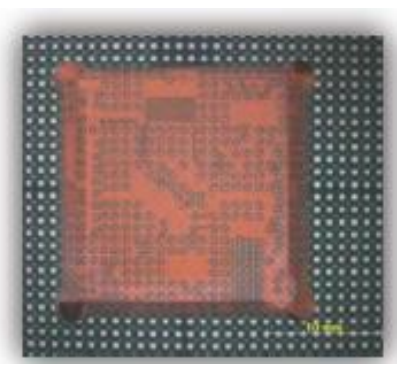
Top Metal. Mag: 200X

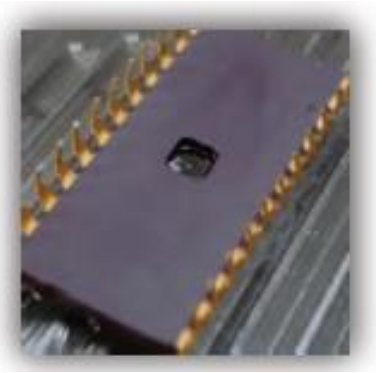


2nd Metal. Mag: 200X



Small Device Deprocessing





Circuit board Ceramic package delayering

CHINWOO TECH
SAMPLE PREP. CENTER

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